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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

SPITTLE, MATTHEW D

ART UNIT PAPER NUMBER

2111

DATE MAILED: 11/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/814,074	Applicant(s) WALKER ET AL.	
	Examiner Matthew D. Spittle	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 November 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 7 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Greeff et al. ('106).

With regard to claim 1, Greeff et al. describe a memory device comprising:

An address bus interface (column 3, lines 34 – 40; Figure 1, item 102);

An address bus termination circuit that can be enabled or disabled (Figure 1, item 120; column 4, lines 21 – 31);

An address bus termination signal input (Figure 1, TERMINATION ENABLE; column 4, lines 21 – 46);

With regard to claim 2, Greeff et al. implicitly describe the address bus termination circuit to be enabled if an asserted address bus termination control signal is received at the address bus termination control signal input since they describe driving the control signal input to where the termination circuit is enabled (column 4, lines 21 – 31). Examiner identifies this as being equivalent to asserting the control signal.

With regard to claim 3, Greeff et al. implicitly describe the address bus termination circuit to be disabled if the address bus termination control signal is not asserted since they describe driving the control signal input to where the termination circuit is disabled (column 4, lines 35 – 46). Examiner identifies this as being equivalent to not asserting the control signal.

With regard to claim 4, Greeff et al. implicitly describe the memory device wherein the address bus termination control signal is asserted when at a logically high voltage level and is not asserted when at a logically low voltage level. Since Greeff et al. describe the invention being used in a digital binary system, there could only be 2 possible values for a particular digital signal – “0” or “1” (column 1, lines 10 – 28), and therefore, Greeff et al. teach all limitations of claim 4. The process of reversing a particular logical signal is old and well known in the art, and therefore designating a particular signal as being asserted when it is logically “high” fails to patentably distinguish over the prior art as evidenced by Janzen et al. (column 2, lines 25 – 33).

With regard to claim 5, Greeff et al. implicitly describe the memory device wherein the address bus termination control signal is asserted when at a logically low voltage level and is not asserted when at a logically high voltage level. Since Greeff et al. describe the invention being used in a digital binary system, there could only be 2 possible values for a particular digital signal – “0” or “1” (column 1, lines 10 – 28), and therefore, Greeff et al. teach all limitations of claim 4. The process of reversing a

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particular logical signal is old and well known in the art, and therefore designating a particular signal as being asserted when it is logically "low" fails to patentably distinguish over the prior art as evidenced by Janzen et al. (column 2, lines 25 – 33).

With regard to claim 6, Greeff et al. describe a memory device further comprising a data bus interface and a data bus termination circuit (data bus: column 3, lines 34 - 40; Figure 1, item 102; data bus termination circuit: Figure 1, item 120; column 4, lines 21 – 31).

With regard to claim 7, Greeff et al. describe a memory device further comprising a data bus termination control signal input, the data bus termination circuit to be enabled in response to an asserted data bus control signal (data bus termination control signal input: Figure 1, TERMINATION ENABLE; column 4, lines 21 – 46).

* * *

Claims 8, 9, 10, 11, 13, 15, 16, and 17 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Greeff et al. ('253).

With regard to claim 8, Greeff et al. describe a memory module comprising:

A plurality of memory devices coupled to an address bus in a daisy chain configuration, each of the plurality of memory devices including:

An address bus interface (Figure 14, item 28; column 4, lines 1 – 6, 25 – 27);

An address bus termination circuit that can be enabled or disabled (Figure 14, item 302; further described in column 9, line 59 – column 10, line 3; column 11, lines 46 – 52);

An address bus termination control signal input (column 9, lines 12 – 24; where a control signal input may be interpreted as a selection signal input).

With regard to claim 9, Greeff et al. describe the memory module wherein for each of the plurality of memory devices the address bus termination circuit is enabled if an asserted address bus termination control signal is received at the address bus termination control signal input (column 9, lines 12 – 24). Examiner identifies the process of the selection signal controlling a switch implicitly comprising the step of the selection signal being asserted, i.e. changed to a logical level that is configured to modify the switch to connect to termination means for that particular memory device.

With regard to claim 10, Greeff et al. describe the memory module wherein for each of the plurality of memory devices the address bus termination circuit is disabled if the address bus termination control signal is not asserted (column 9, lines 12 – 24). Examiner identifies the process of the selection signal controlling a switch implicitly comprising the step of the selection signal being not asserted, i.e. changed to a logical level that is configured to modify the switch to disconnect the termination means for that particular memory device.

With regard to claim 11, Greeff et al. implicitly describe the memory module wherein for each of the plurality of memory devices the address bus termination control signal is asserted when at a logically high voltage level and is not asserted when at a logically low voltage level. Since Greeff et al. describe the invention being used in a digital binary system, there could only be 2 possible values for a particular digital signal – “0” or “1” (column 1, lines 10 – 28), and therefore, Greeff et al. teach all limitations of claim 4. The process of reversing a particular logical signal is old and well known in the art, and therefore designating a particular signal as being asserted when it is logically “high” fails to patentably distinguish over the prior art as evidenced by Janzen et al. (column 2, lines 25 – 33).

With regard to claim 13, Greeff et al. implicitly describe the memory module wherein for each of the plurality of memory devices the address bus termination control signal is asserted when at a logically low voltage level and is not asserted when at a logically high voltage level. Since Greeff et al. describe the invention being used in a digital binary system, there could only be 2 possible values for a particular digital signal – “0” or “1” (column 1, lines 10 – 28), and therefore, Greeff et al. teach all limitations of claim 4. The process of reversing a particular logical signal is old and well known in the art, and therefore designating a particular signal as being asserted when it is logically “low” fails to patentably distinguish over the prior art as evidenced by Janzen et al. (column 2, lines 25 – 33).

With regard to claim 15, Greeff et al. describe a memory module wherein each of the plurality of memory devices (Figure 14, items 54, 56, 60) further includes a data bus interface and a data bus termination circuit (column 4, lines 1 – 6; data bus interface: Figure 14, item 28; data bus termination circuit: Figure 14, item 302; ; column 9, line 59 – column 10, line 3; column 11, lines 46 – 52).

With regard to claim 16, Greeff et al. describe a memory module wherein each of the plurality of memory devices further includes a data bus termination control signal input, the data bus termination circuit to be enabled in response to an asserted data bus termination control signal (where a data bus termination control signal may be interpreted as a selection signal for controlling the two-way switches; column 9, lines 12 – 24).

With regard to claim 17, Greeff et al. describe a method comprising:

Connecting in a daisy chain configuration an address bus to a plurality of memory devices on a memory module (Figure 14, item 28; column 4, lines 1 – 6, 25 – 27);;

Providing address bus termination circuitry in the plurality of memory devices (Figure 14, item 302; further described in column 11, lines 46 – 52);

Enabling the address bus termination circuitry of only one of the plurality of memory devices. Greeff et al. provide no reason as to why their invention would not be capable of enabling the termination circuitry for only a single memory device, and

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therefore describe this limitation (Figure 14, item 302; column 9, line 59 – column 10, line 3; column 11, lines 46 – 52).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 12, 14, 18, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greeff et al. ('253) in view of Gasbarro.

With regard to claim 12, Greeff et al. teach a plurality of memory devices in a daisy chain configuration (column 4, lines 25 – 27) but fail to teach all but the last memory device having its address bus termination control signal input tied to ground and the last memory device having its address bus termination control signal tied to a positive voltage.

Gasbarro teaches teach all but the last memory device having its address bus termination control signal input tied to ground and the last memory device having its address bus termination control signal tied to a positive voltage (column 5, lines 4 – 8, 33 – 41, 55 – 57, 63 – 66; column 6, lines 20 – 25, 32 – 54; column 7, lines 6 – 14). Gasbarro is silent as to the explicit voltage level of the address bus termination control signal input, however one of ordinary skill in this art would recognize that in digital system, device inputs can be “active high” or “active low”, and using either to enable or disable the termination circuit is obvious and well known in the art as evidenced by Janzen et al. (column 2, lines 25 – 33).

With regard to claim 14, Greeff et al. teach a plurality of memory devices in a daisy chain configuration (column 4, lines 25 – 27) but fail to teach all but the last memory device having its address bus termination control signal input tied to a positive voltage and the last memory device having its address bus termination control signal tied to ground.

Gasbarro teaches teach all but the last memory device having its address bus termination control signal input tied to a positive voltage and the last memory device having its address bus termination control signal tied ground (column 5, lines 4 – 8, 33 – 41, 55 – 57, 63 – 66; column 6, lines 20 – 25, 32 – 54; column 7, lines 6 – 14). Gasbarro is silent as to the explicit voltage level of the address bus termination control signal input, however one of ordinary skill in this art would recognize that in digital system, device inputs can be “active high” or “active low”, and using either to enable or

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disable the termination circuit is obvious and well known in the art as evidenced by Janzen et al. (column 2, lines 25 – 33).

With regard to claim 18, Greeff et al. teach a plurality of memory devices in a daisy chain configuration (column 4, lines 25 – 27), but fail to teach enabling the address bus termination circuitry of only the last memory.

Gasbarro teach enabling the address bus termination circuitry of the last memory device (column 5, lines 55 – 57; column 6, lines 20 – 25; column 7, lines 6 – 14).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to combine the method of Gasbarro with the method of Greeff et al. in order to minimize signal travel time between the memory controller and memory devices (column 5, lines 33 – 41), as well as prevent signal reflections on the bus (column 7, lines 6 – 14).

With regard to claim 19, Greeff et al. teach the additional limitation of enabling the last memory device in the daisy chain configuration by coupling an address bus termination control pin to a positive voltage (where an address bus termination control pin may be interpreted as a selection signal input; column 9, lines 12 – 24; column 11, lines 40 – 52). Greeff et al. is silent as to the polarity of the voltage applied to the pin, however, one of ordinary skill in this art would recognize that in a digital system, device inputs can be “active high” or “active low”, and using either to enable or disable the

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termination circuit is obvious and well known in the art as evidenced by Janzen et al. (column 2, lines 25 – 33).

With regard to claim 20, Gasbarro teaches the additional limitation wherein enabling the address bus termination circuitry of only one of the plurality of memory devices includes disabling the address bus termination circuits in all but the last memory device in the daisy chain configuration by coupling address bus termination control pins on all but the last memory device to ground (column 5, lines 4 – 8, 33 – 41, 55 – 57, 63 – 66; column 6, lines 20 – 25, 32 – 54; column 7, lines 6 – 14). Gasbarro is silent as to the explicit voltage level of the address bus termination control pins, however one of ordinary skill in this art would recognize that in digital system, device inputs can be “active high” or “active low”, and using either to enable or disable the termination circuit is obvious and well known in the art as evidenced by Janzen et al. (column 2, lines 25 – 33).

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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11/8/05